

MS-7309

uATX(244mm X 205mm)

CPU:

AMD AM2 Socket940

System Chipset:

North Bridge --- MCP61-P/S/V

South Bridge --- NA

OnBoard Chipset:

Clock Gen:NA

AC'97 Codec:ALC861/883, Azalia 8 channel codec(with 1 SPDIF out)

LAN(PHY):Realtek RT8201CL(10/100)/Realtek RT8211B(Giga)

SIO:Fintek 882(with smart fan control-3/4 pin co-lay)

Flash ROM:4MB SPI

IEEE 1394:VIA VT6307 /VT6308

Main Memory:

DDRII (400/533/667/800MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

PCI Slot * 2

PWM:

Controller:ISL6566CRZ (3-Phase)

ACPI:

WINBOND / MS6 Ver: RBF

Other:

IDE(DMA133) *1

FDD *1

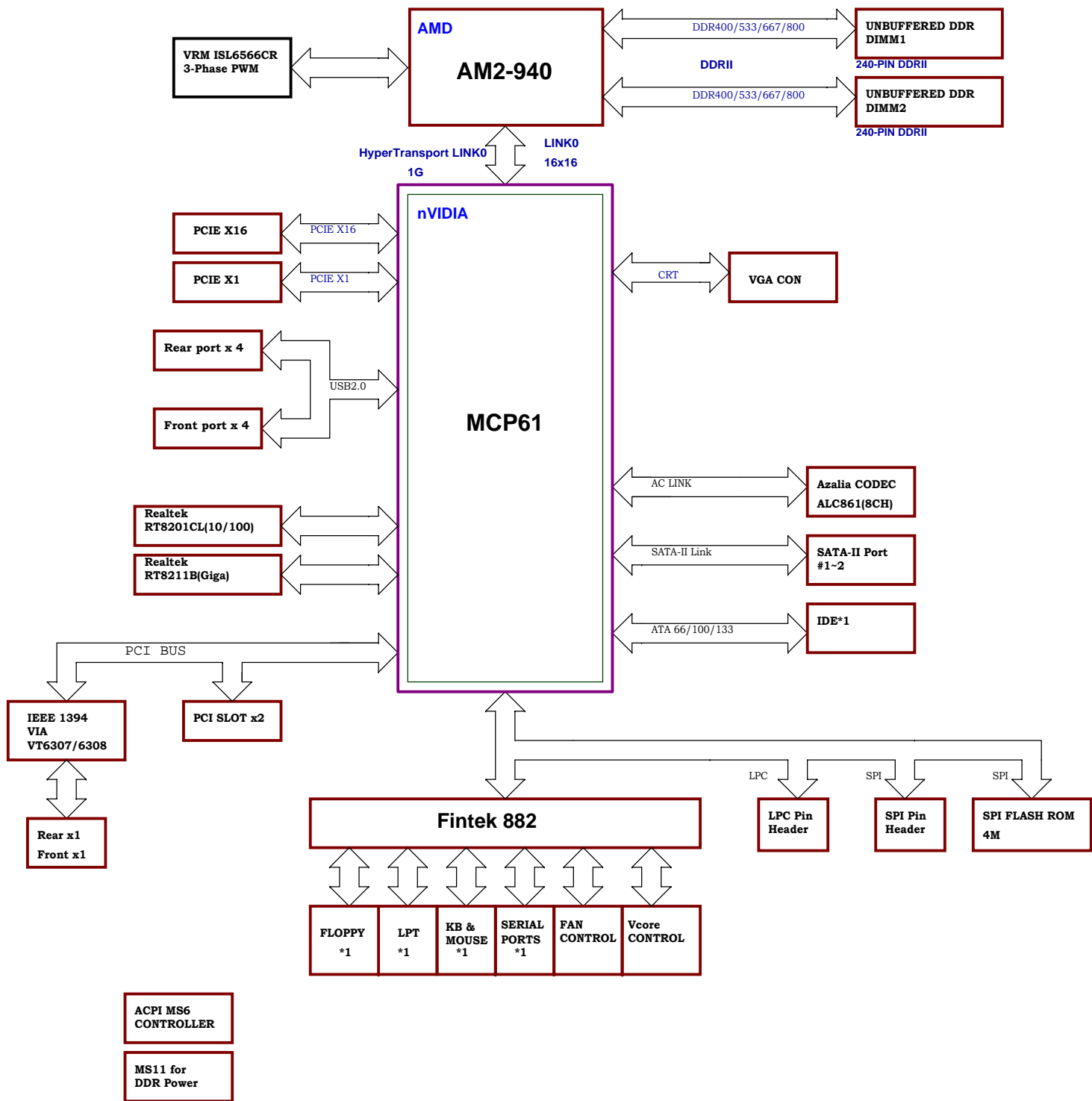
SATA(SATA2-300MB/S) *2

USB2.0 *8(Rear*4 Front*4)

COM PORT *1

LPT PORT *1

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PCI RESET DEVICE

MCP61	
Signals	Target
PCI_RESET0*	PCISLOT1
PCI_RESET1*	PCISLOT2
PCI_RESET2*	MS6
PCI_RESET3*	1394
LPC_RESET*	LPC/SIO

MS6	
Signals	Target
HDD_RST#	IDE

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 2 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#Y PCI_INT#Z PCI_INT#W PCI_INT#X	PCI_REQ1# PCI_GNT1#	AD26	PCI_CLKSLOT1 (PCICLK1)
PCI Slot 2	PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W	PCI_REQ2# PCI_GNT2#	AD25	PCI_CLKSLOT2 (PCICLK2)
IEEE1394	PCI_INT#Z	PCI_REQ0# PCI_GNT0#	AD24	PCICLK_1394 (PCICLK0)
LPC				LPC_PCLK
SIO				SIO_PCLK

CPU VID TABLE	
VID	VOLTAGE
00000	1.5500V
00001	1.5250V
00010	1.5000V
00011	1.4750V
00100	1.4500V
00101	1.4250V
00110	1.4000V
00111	1.3750V
01000	1.3500V
01001	1.3250V
01010	1.3000V
01011	1.2750V
01100	1.2500V
01101	1.2250V
01110	1.2000V
01111	1.1750V
10000	1.1500V
10001	1.1250V
10010	1.1000V
10011	1.0750V
10100	1.0500V
10101	1.0250V
10110	1.0000V
10111	0.9750V
11000	0.9500V
11001	0.9250V
11010	0.9000V
11011	0.8750V
11100	0.8500V
11101	0.8250V
11110	0.8000V
11111	0.7750V

USB

	Port	DATA +/-	OC#
Rear	USB1	USB0- USB0+ USB1- USB1+	USB_OC#0 (OC#0~1)
	LAN_USB1	USB2- USB2+ USB3- USB3+	USB_OC#2 (OC#2~3)
Front	JUSB1	USB4- USB4+ USB5- USB5+	USB_OC#4 (OC#4~5)
	JUSB2	USB6- USB6+ USB7- USB7+	USB_OC#6 (OC#6~7)

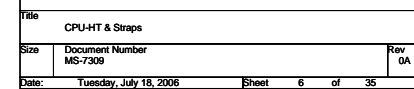
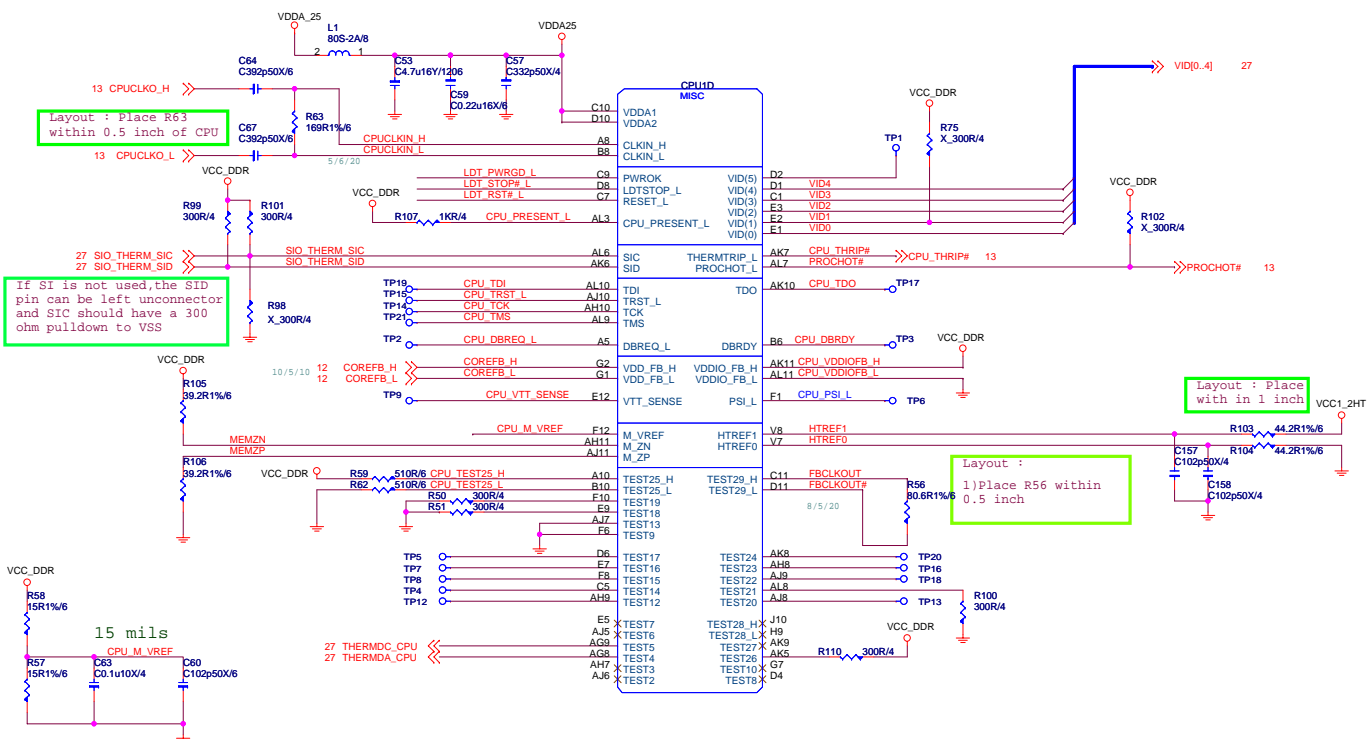
MCP61 GPIO TABLE

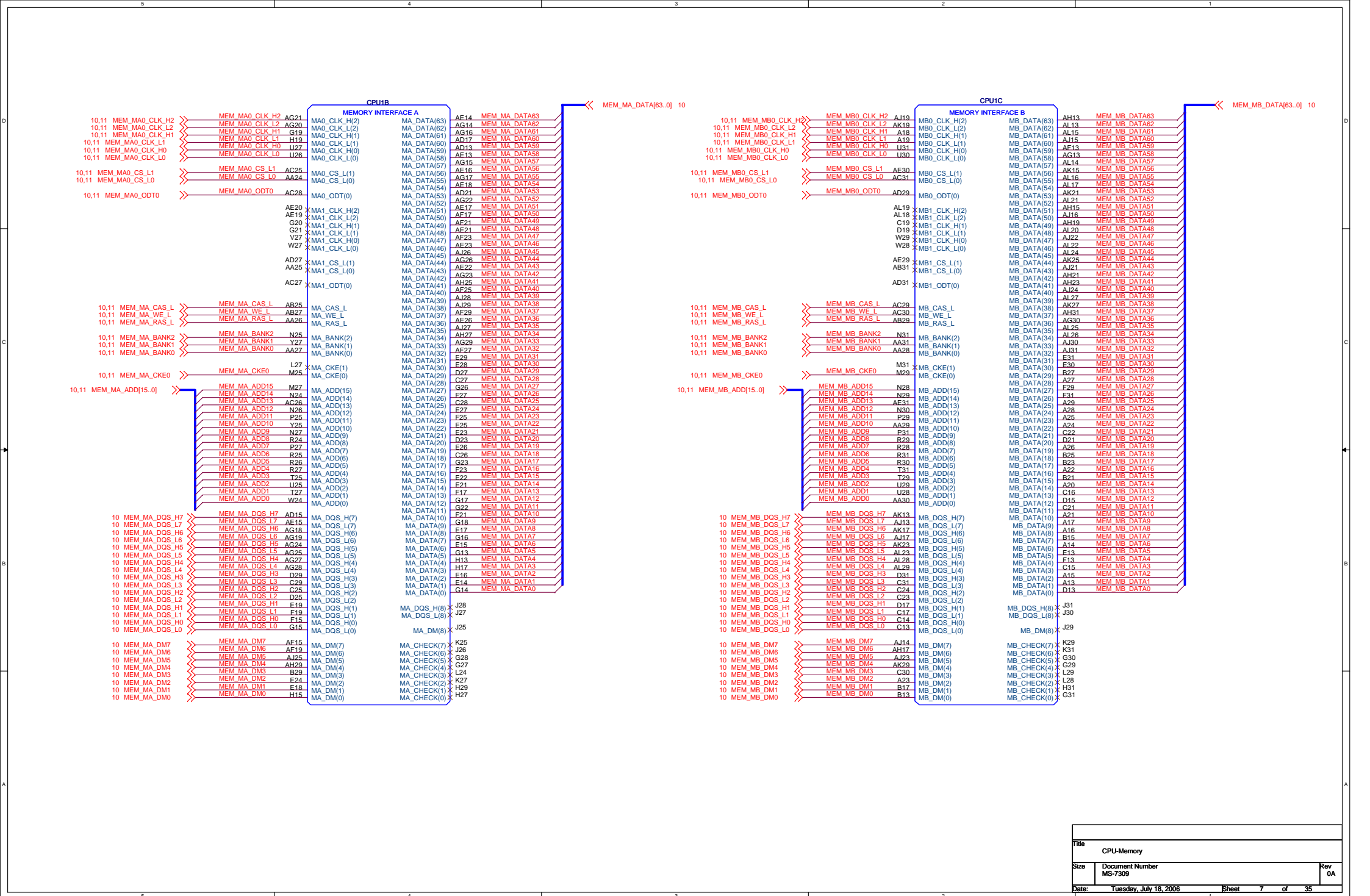
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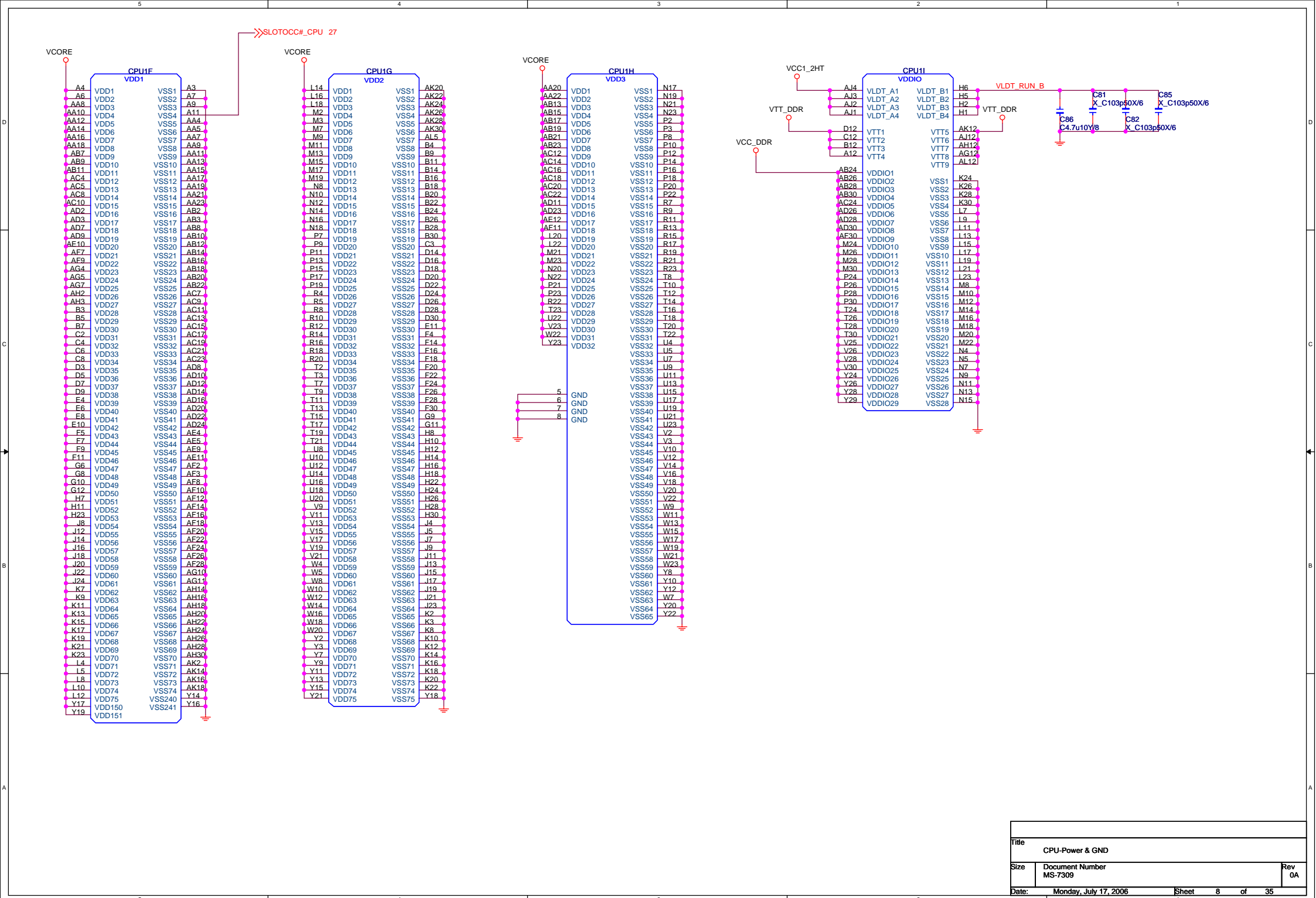
SIO GPIO TABLE

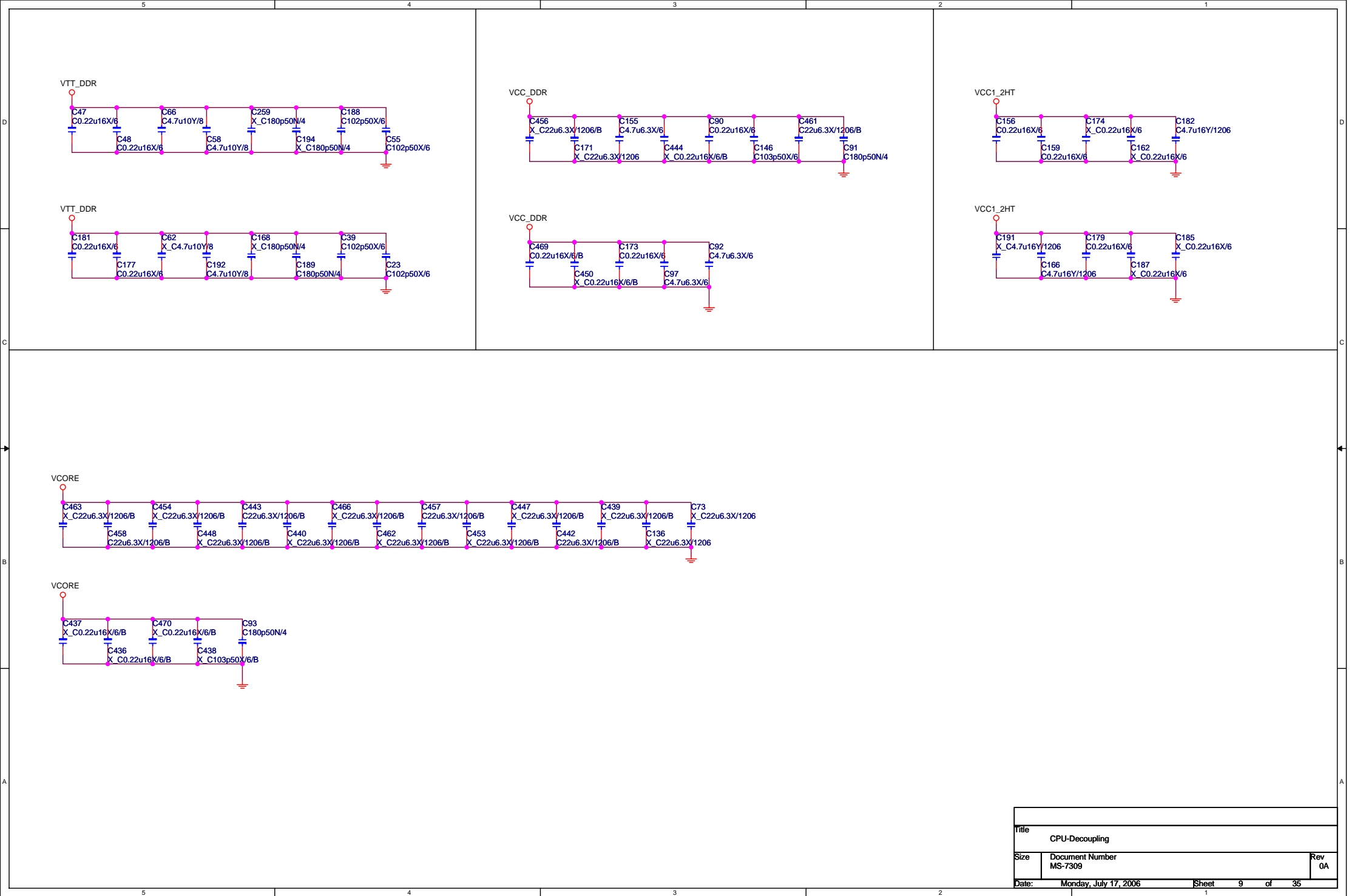
GROUP	PIN NAME	FUNCTION
UART & SIR	IRTX/GPIO42 IRRX/GPIO43 GPIO17	-- -- --
Hardware Monitor	FANIN3/GPIO40 FAN_CTL3/GPIO41 PME#/GPIO25 GPIO10/SPISLK/FININ4 GPIO11/SP1_CS0#/FAN_CTL4 FPIO12/SP1_MISO/FANCTL1_1 GPIO13/SP1_MOSI/BEEP GPIO14/FWH_DIS/WDTRST#/SP1_CS1#	-- -- PME# SP1_SLK SP1_CS0# SP1_MISO SP1_MOSI SP1_CS1#
ACPI Function Pins	GPIO15/LED_VSB/ALERT# GPIO16/LED_VCC_Turbo2# PCIRST1#/GPIO20 PCIRST2#/GPIO21 PCIRST3#/GPIO22 GPIO23/RSTCON# ATXPG_IN/GPIO24 PWROK/GPIO32 PWSIN#/GPIO26 PWSOUT#/GPIO27 S3#/GPIO30 PSON#/GPIO31 RSMRST#/GPIO33	-- CPU_FAN_GPO -- -- -- -- ATXPG_IN -- PWSIN# PWSOUT# S3# PSON# --
VID Controller	VIDOUT0/GPIO0 VIDOUT1/GPIO1 VIDOUT2/GPIO2 VIDOUT3/GPIO3 VIDOUT4/GPIO4 VIDOUT5/GPIO5/SIC SLOT0CC#/GPIO6 GPIO77/Turbo1#/WDTRST#	VIDOUT0 VIDOUT1 VIDOUT2 VIDOUT3 VIDOUT4 SIC SLOT0CC# --

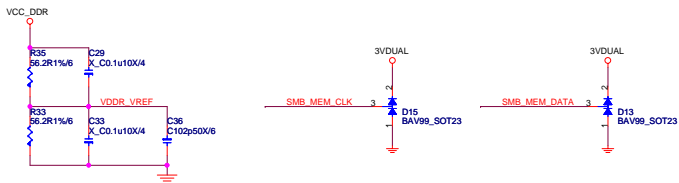
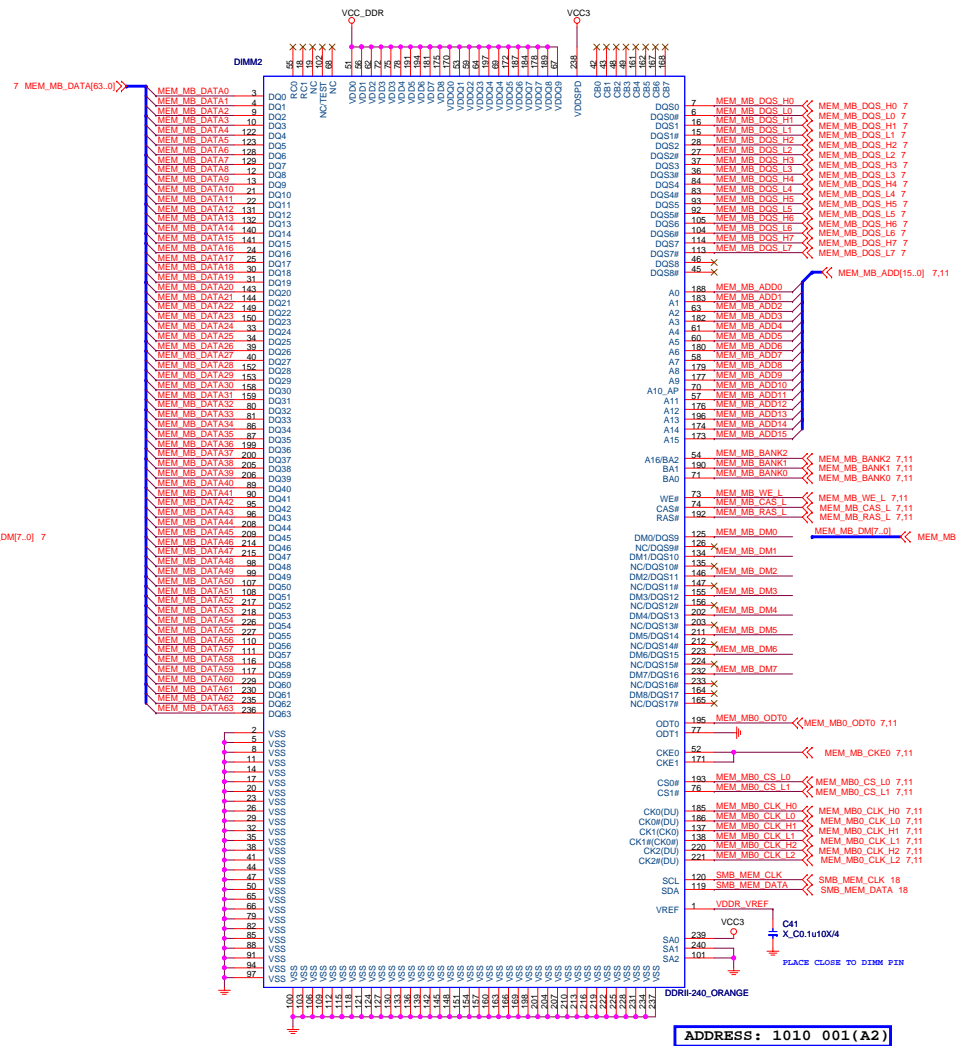
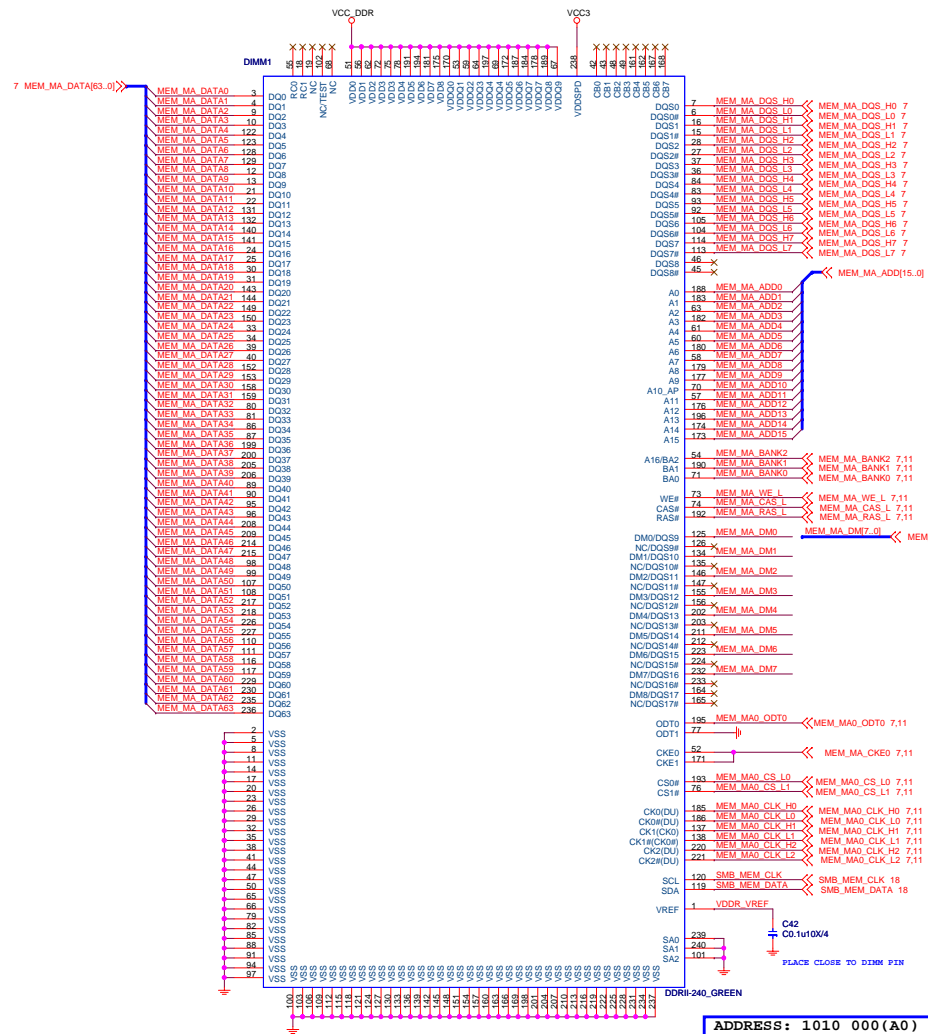
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GPIO Table			
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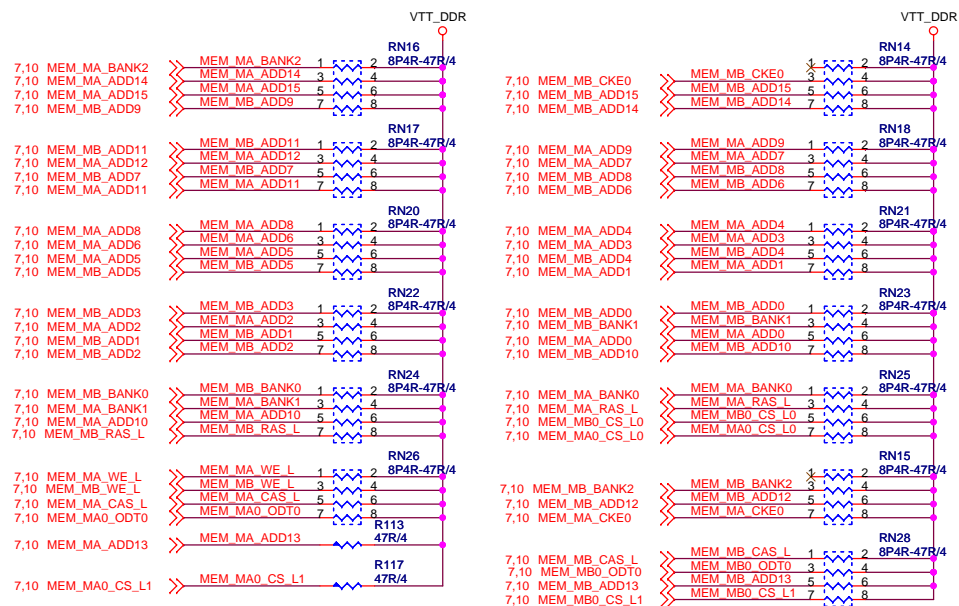




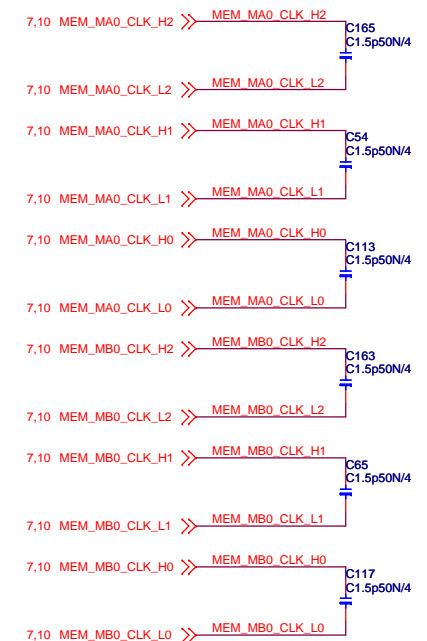
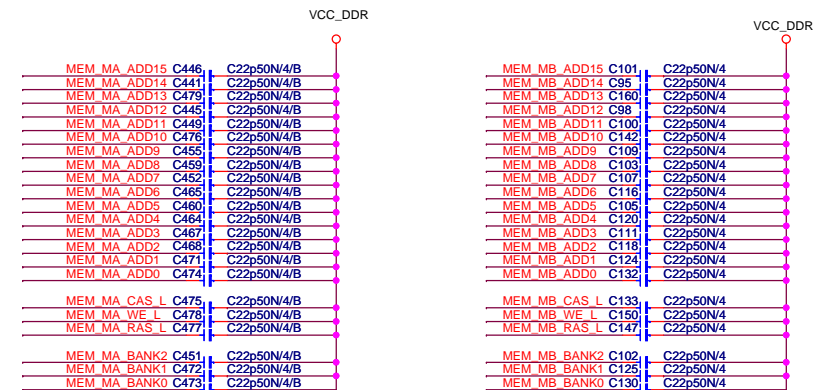




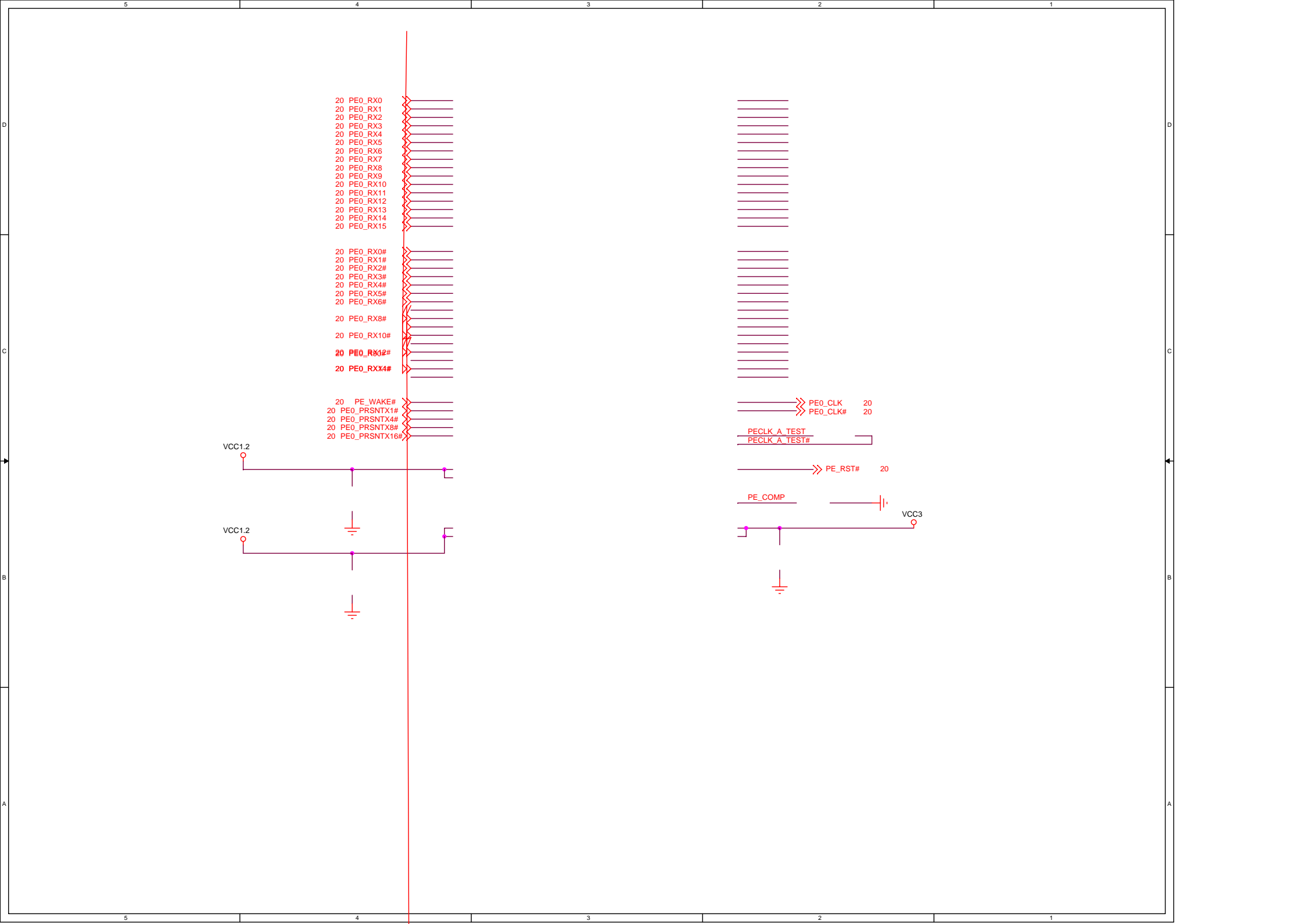
RTT:Place Behind DIMMs

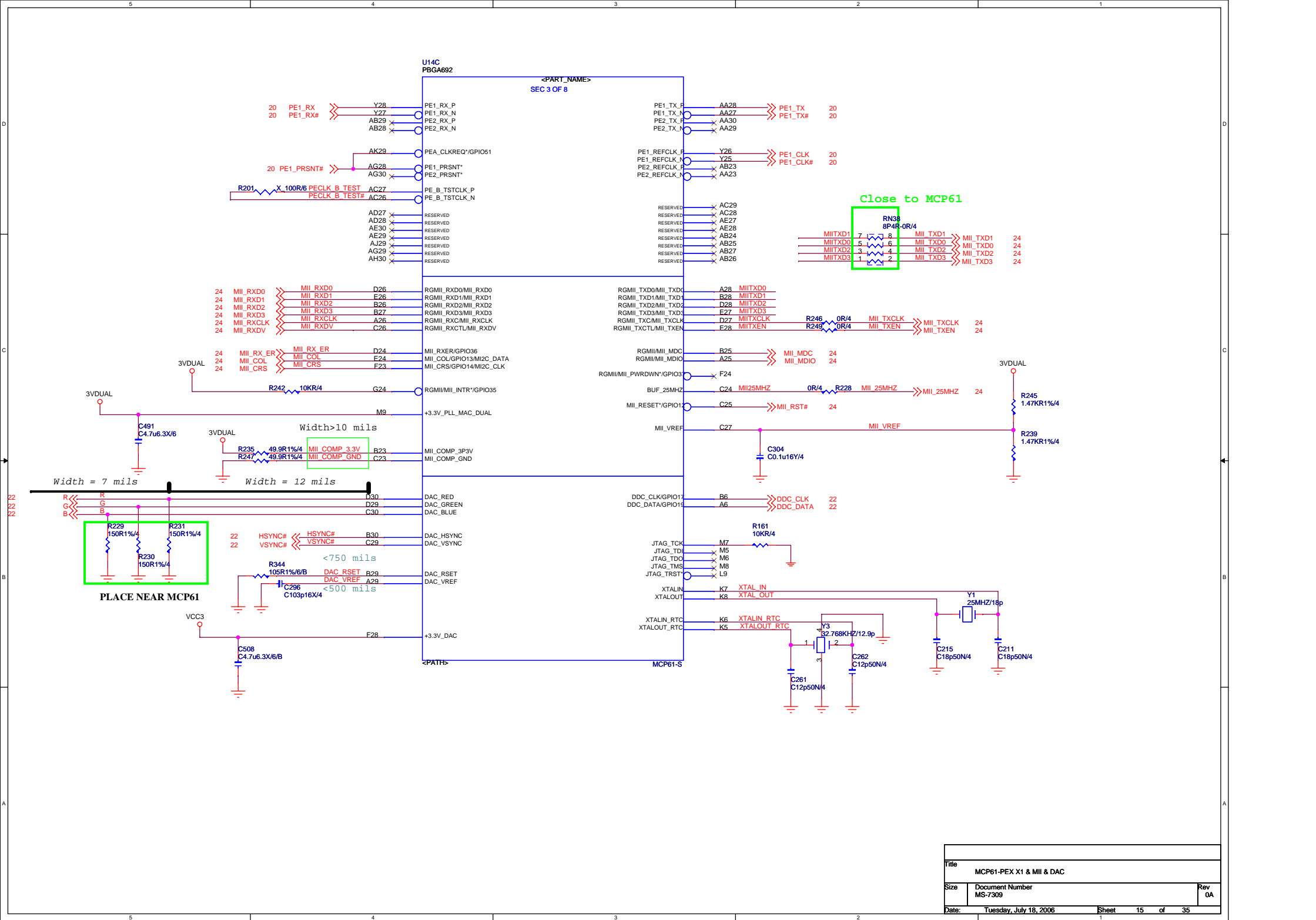


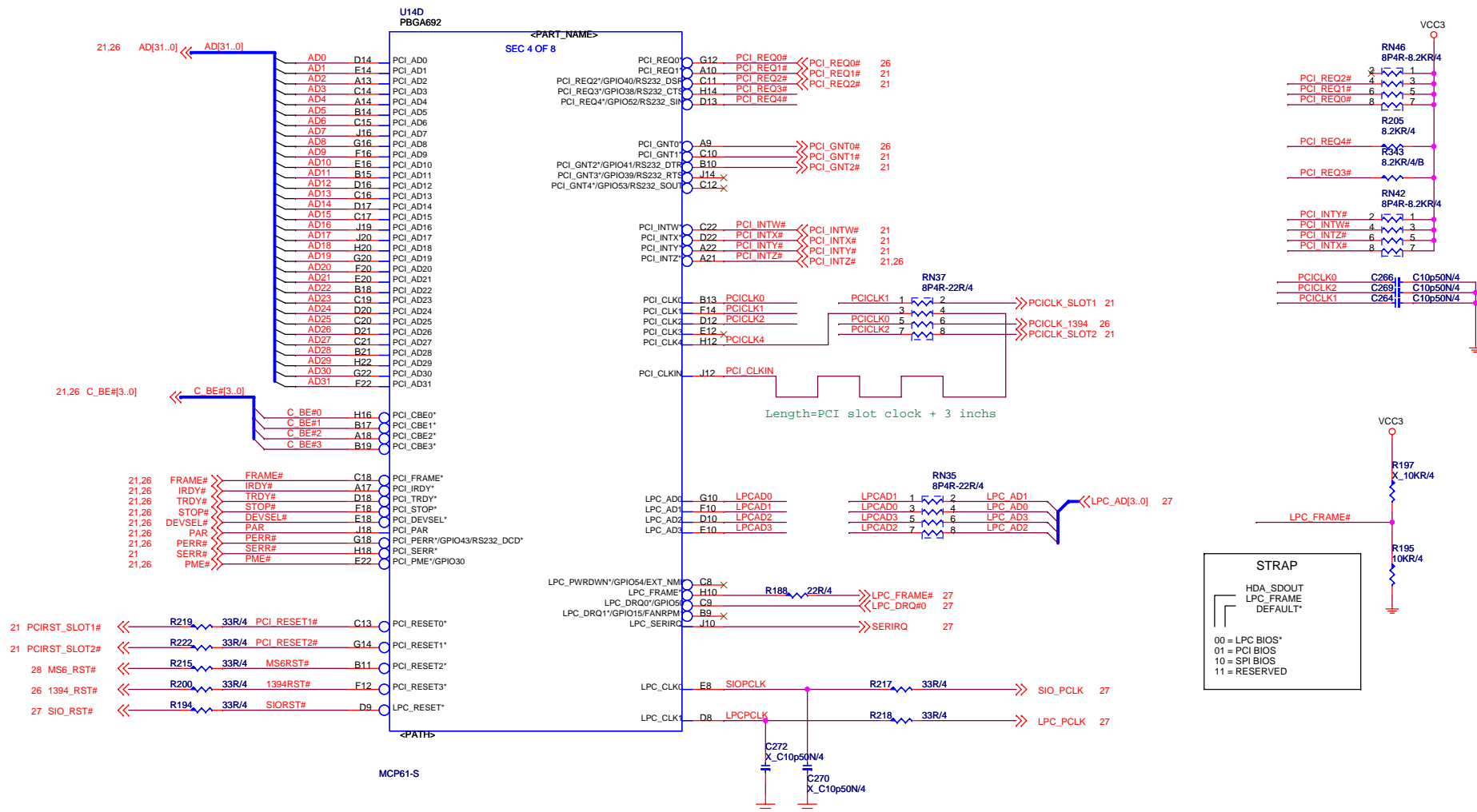
Place Between Processor and DIMMs



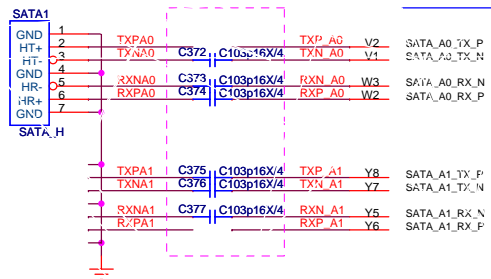
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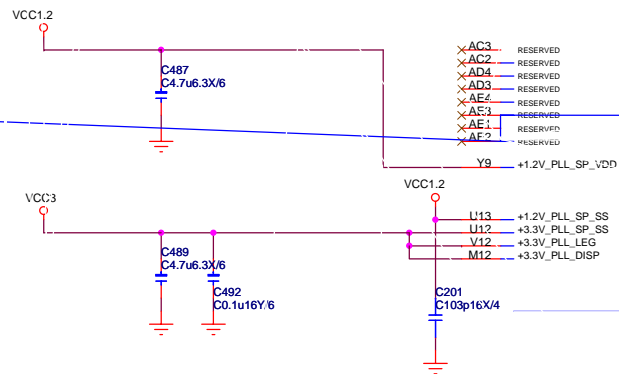
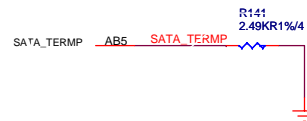
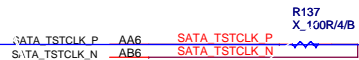
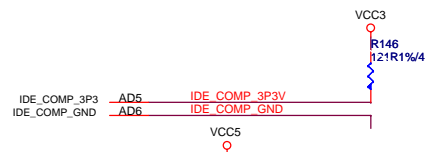
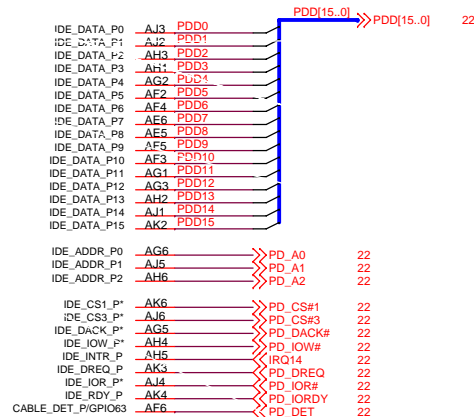


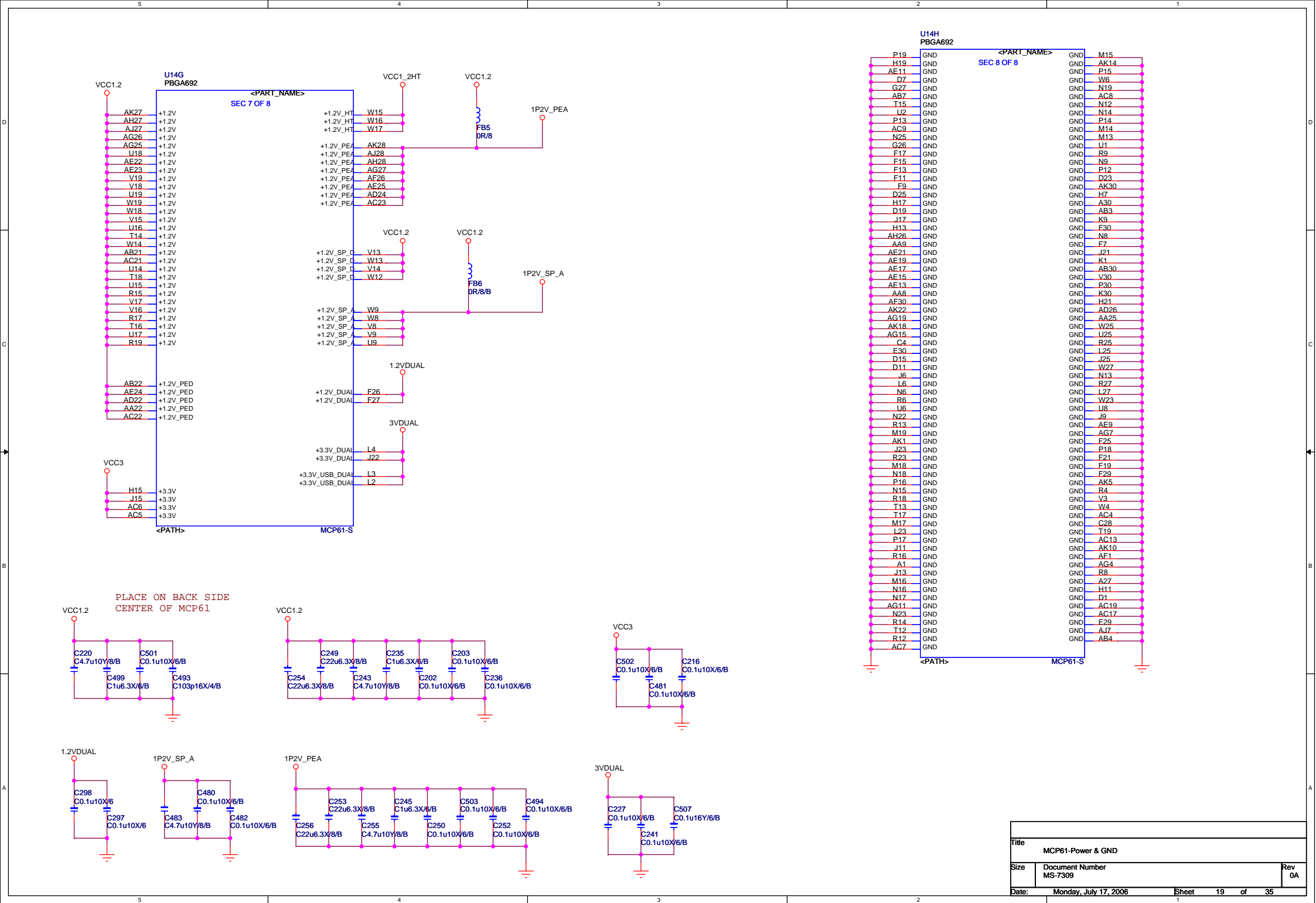
Near SATA CONNECTOR



X Y4 SATA_B0_TX_P
 X Y3 SATA_B0_TX_N
 X AA4 SATA_B0_RX_N
 X AA3 SATA_B0_RX_P

X AA2 SATA_B1_TX_P
 X AA1 SATA_B1_TX_N
 X AB1 SATA_B1_RX_N
 X AB2 SATA_B1_RX_P

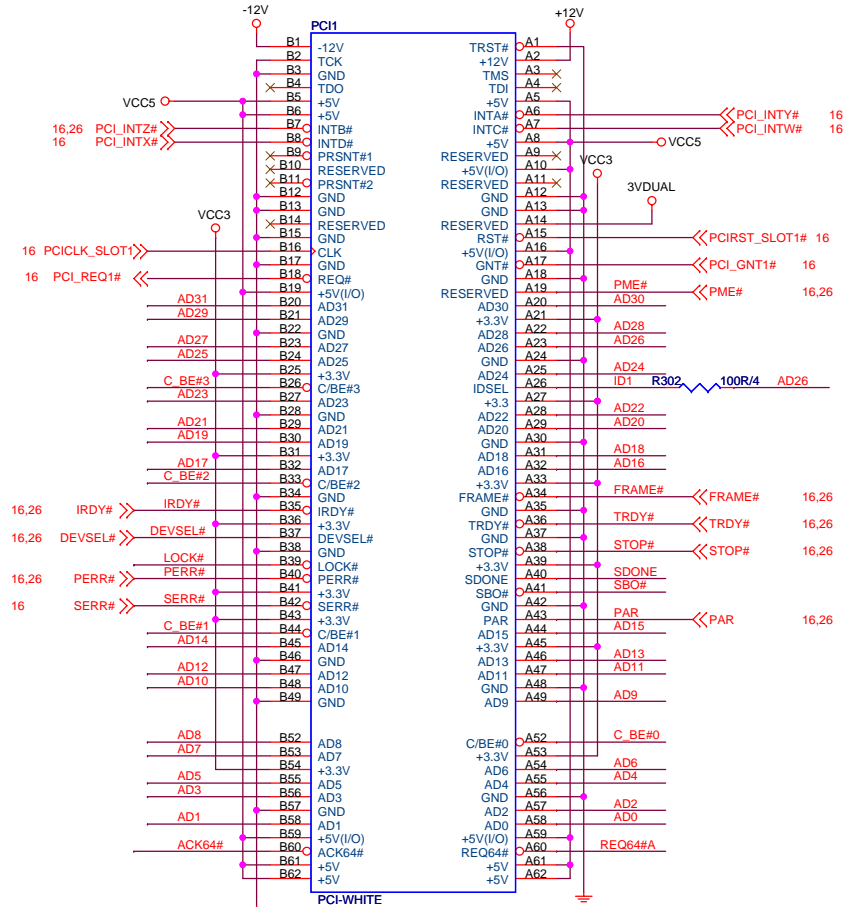




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MCP61-Power & GND		
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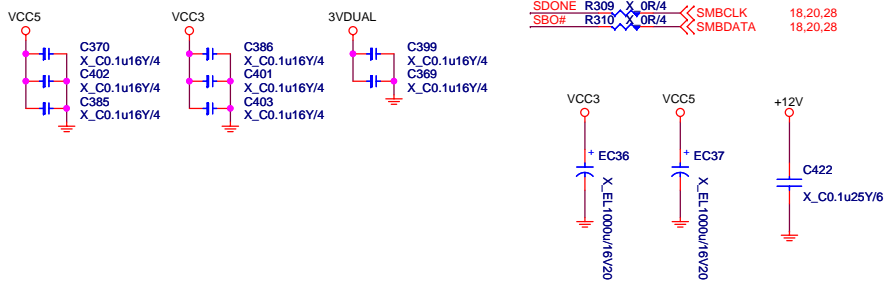
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

16,26 AD[31..0] >> AD[31..0]
16,26 C_BE#[3..0] >> C_BE#[3..0]



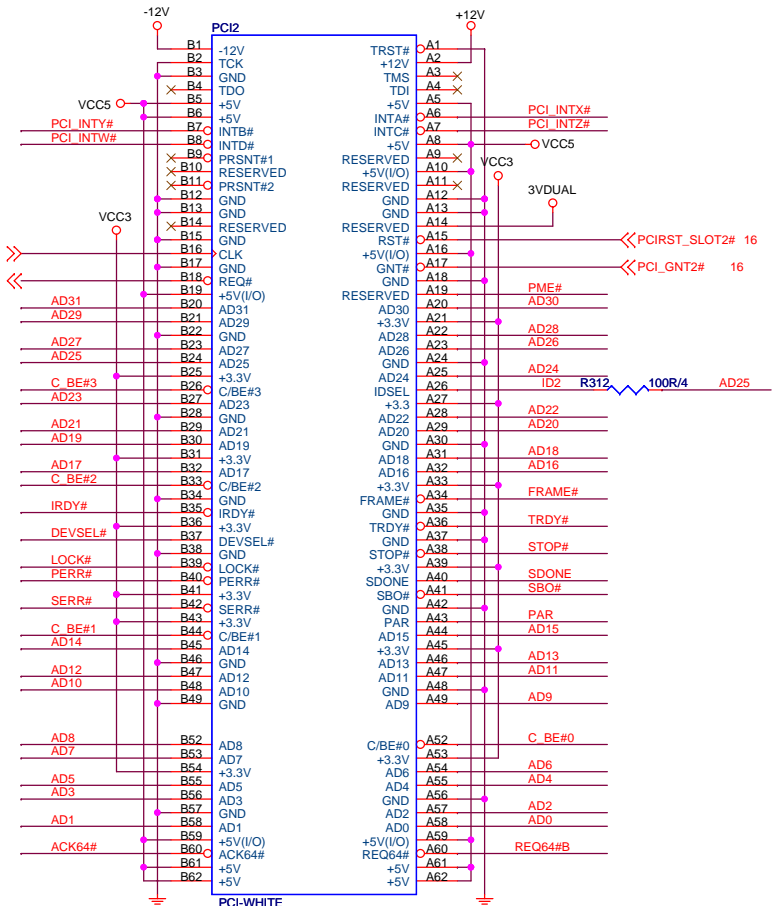
IDSEL = AD26
PCI_REQ1# PCI_GNT1#
INT Y# Z# W# X#
PCICLK_SLOT1

PCI SLOT DECOUPLING CAPACITORS



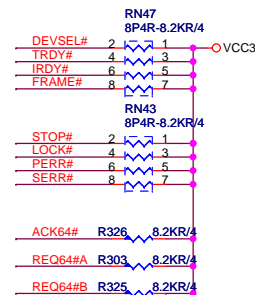
PCI SLOT 2 (PCI VER: 2.2 COMPLY)

16 PCICLK_SLOT2 >> PCICLK_SLOT2
16 PCI_REQ2# >> PCI_REQ2#



IDSEL = AD25
PCI_REQ2# PCI_GNT2#
INT X# Y# Z# W#
PCICLK_SLOT2

PCI PULL-UP / DOWN RESISTORS



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PCI CONN 1&2		
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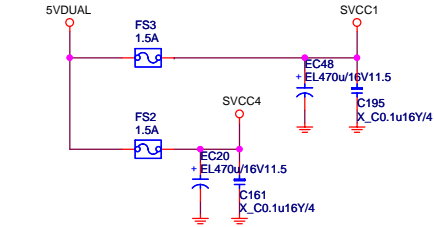
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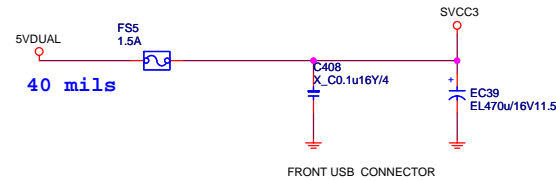
POWER CIRCUIT FOR USB PORT 0,1,2,3

40 mils



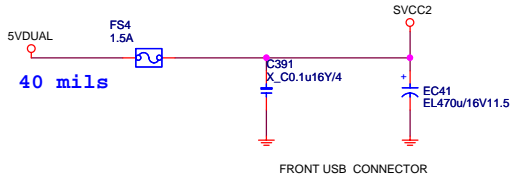
POWER CIRCUIT FOR USB PORT 4,5

40 mils

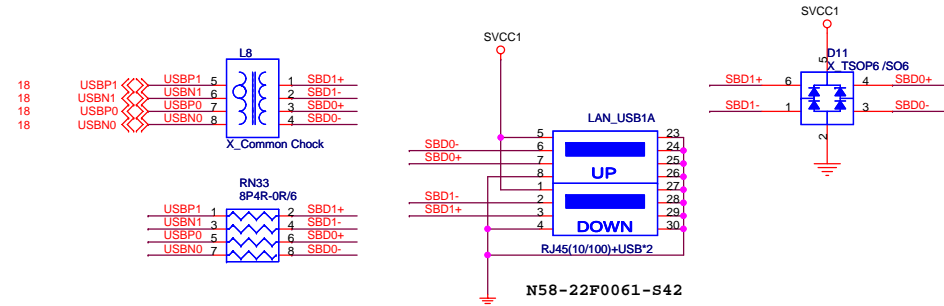


POWER CIRCUIT FOR USB PORT 6,7

40 mils



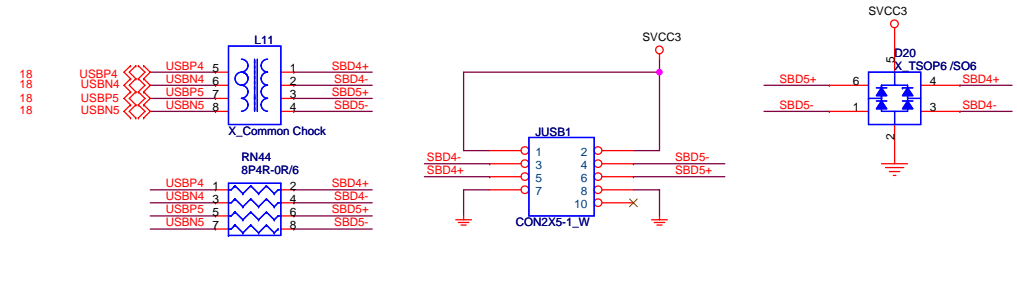
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

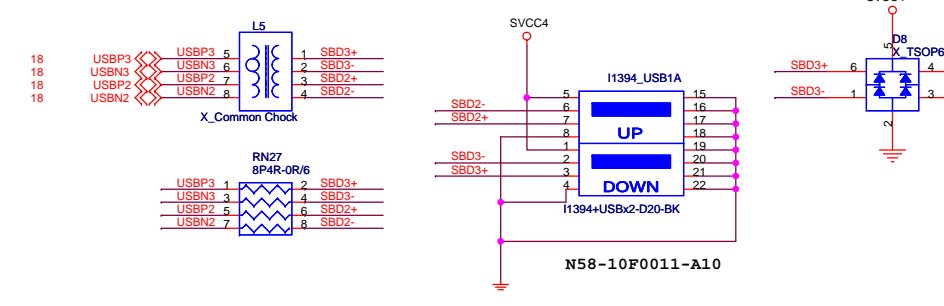
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

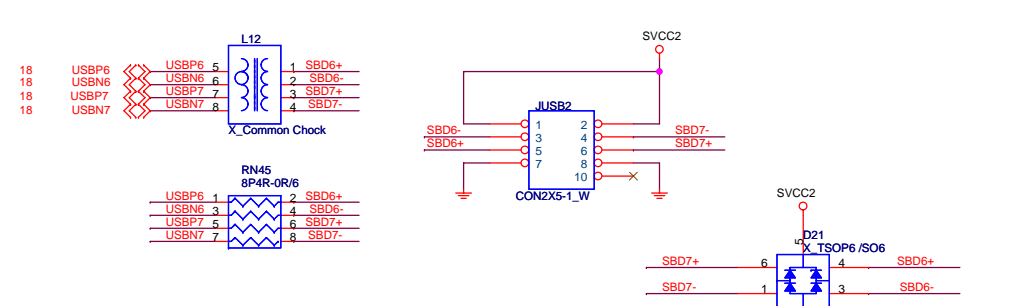
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

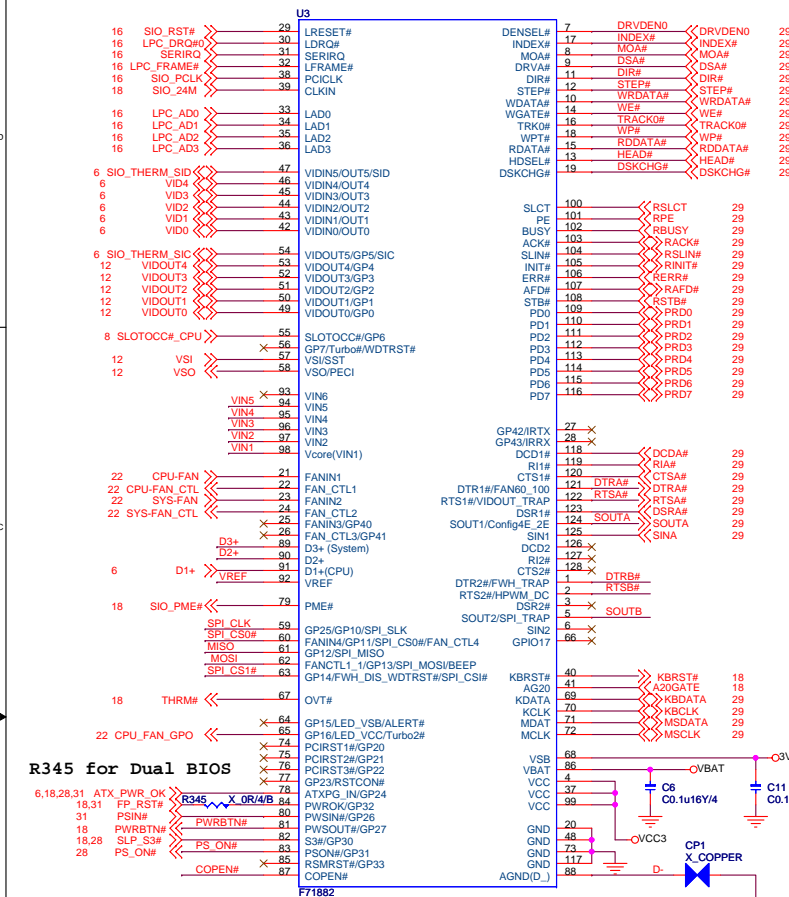
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



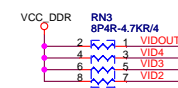
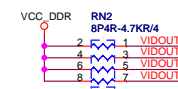
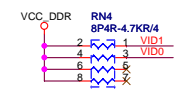
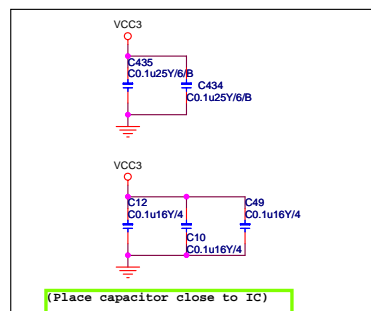
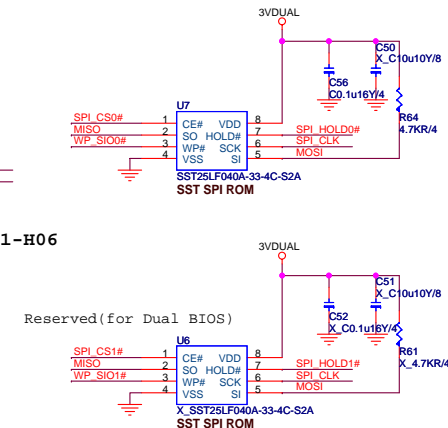
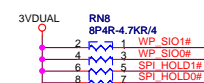
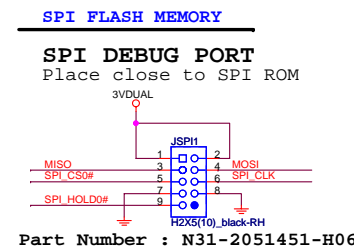
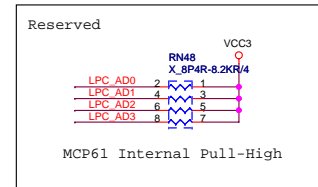
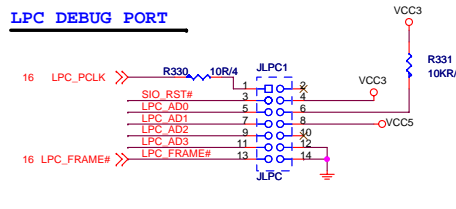
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

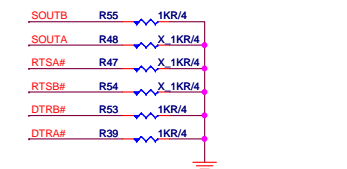
LPC SUPER I/O F71882



LPC DEBUG PORT



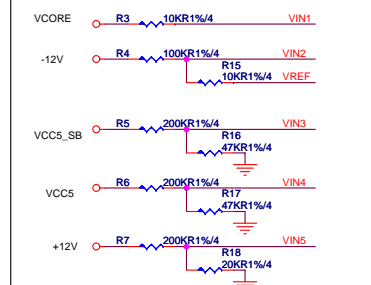
POWER TRIP R



	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
SOUTB/DTRB#	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

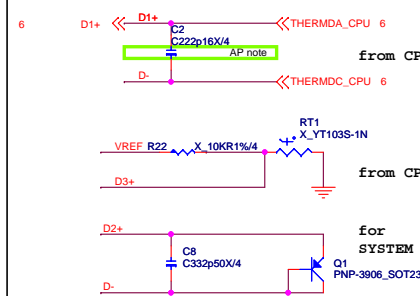
VOLTAGE SENSING(H/W Monitor).

The best voltage input level is about 1V.

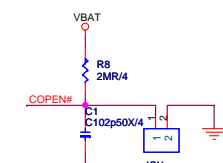


Temperature Sensing

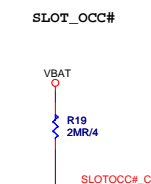
DIODE SENSING CIRCUIT



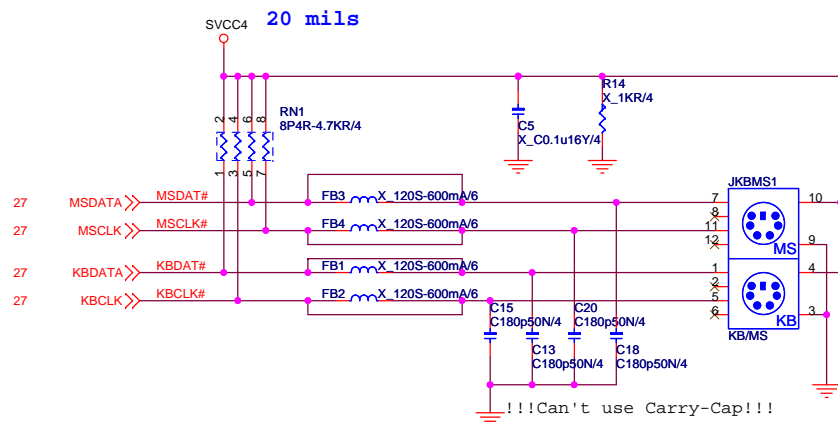
CASE OPEN CIRCUIT



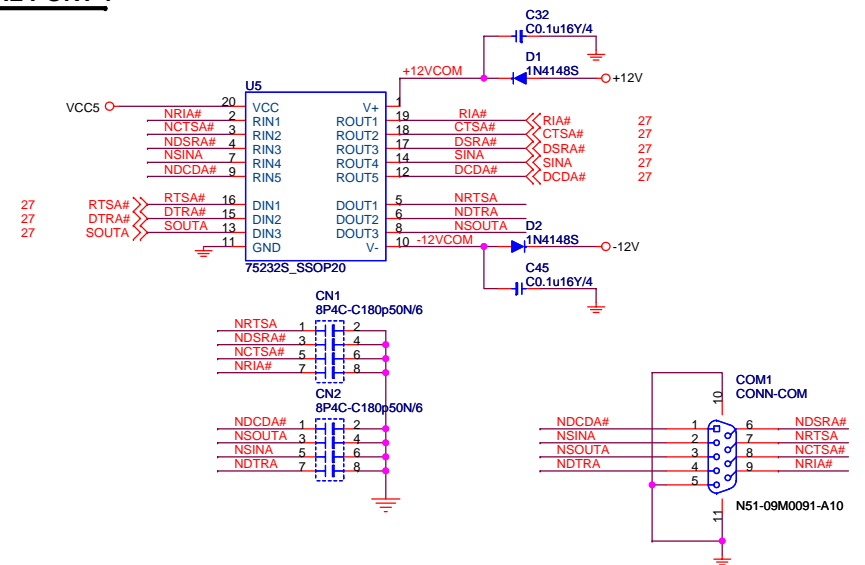
CPU VID reset



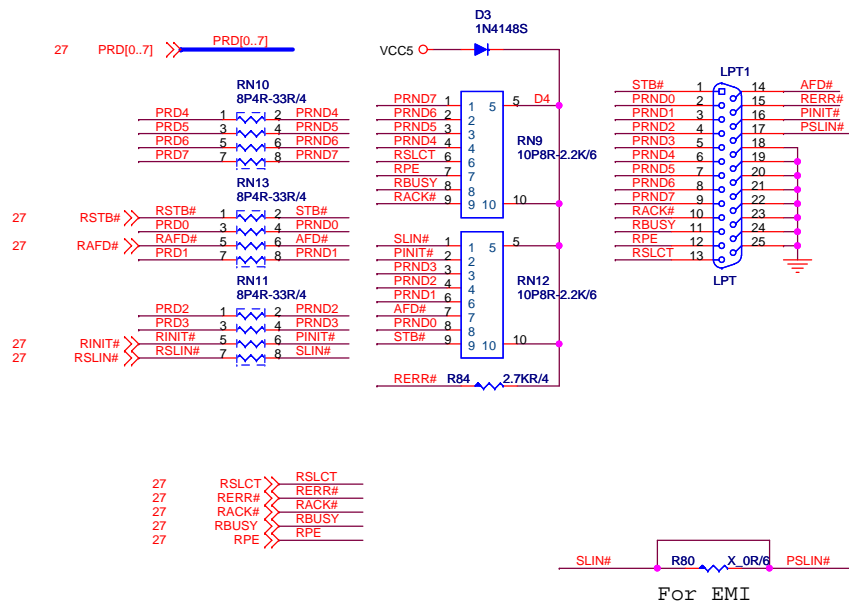
PS2 KEYBOARD & MOUSE CONNECTOR



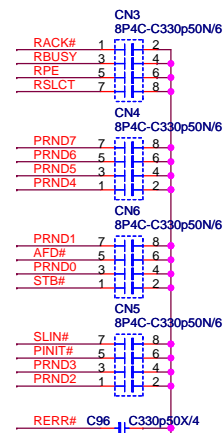
SERIAL PORT 1



PARALLAL PORT

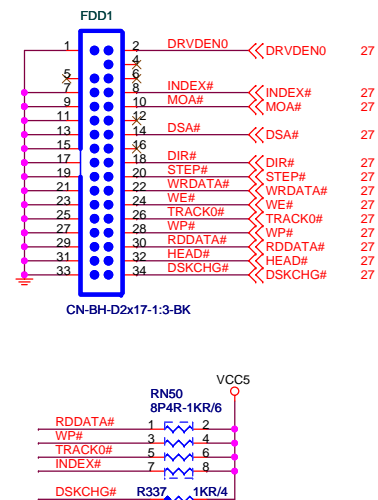


For EMI

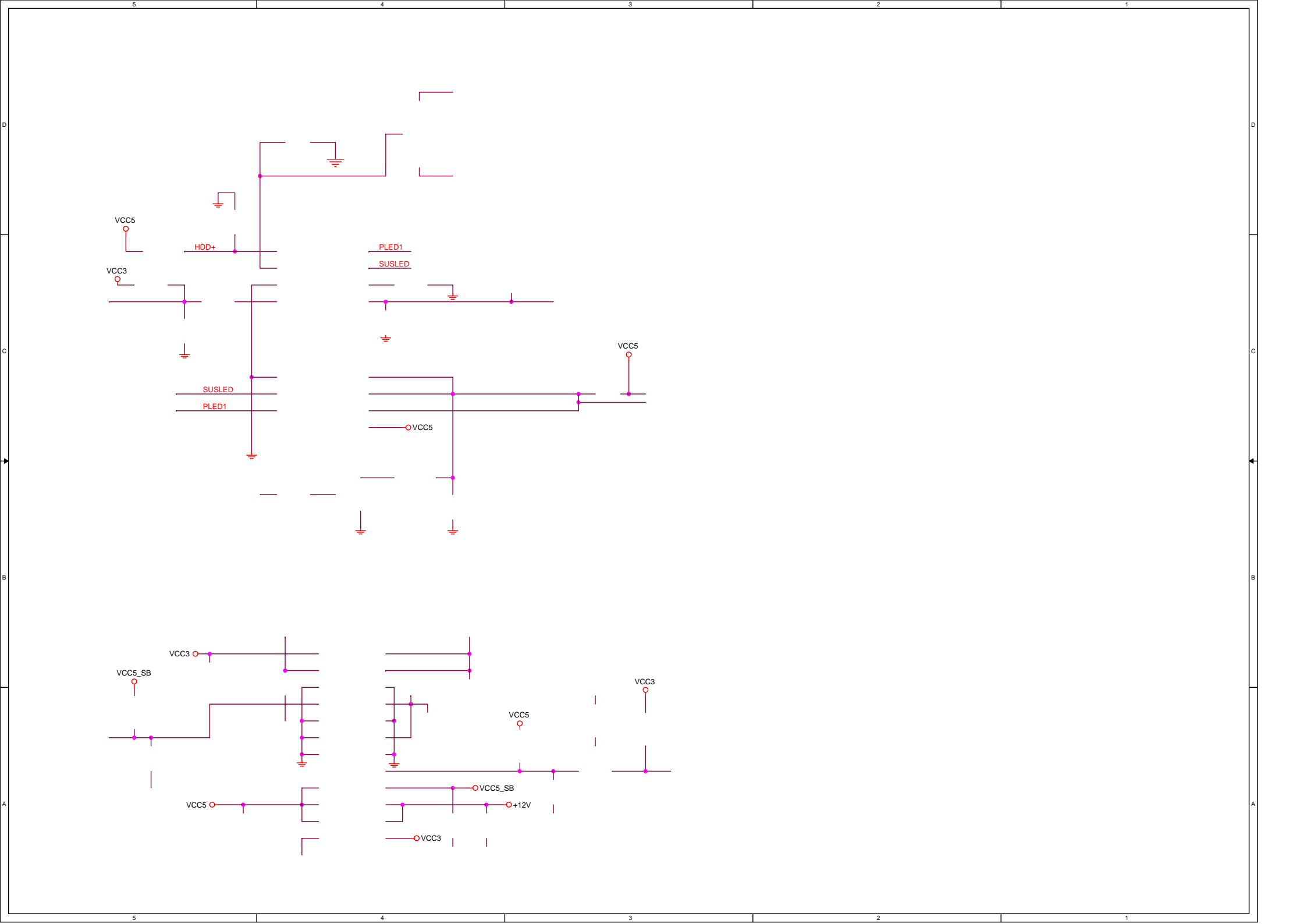


For EMI

FLOPPY CONN BOLCK

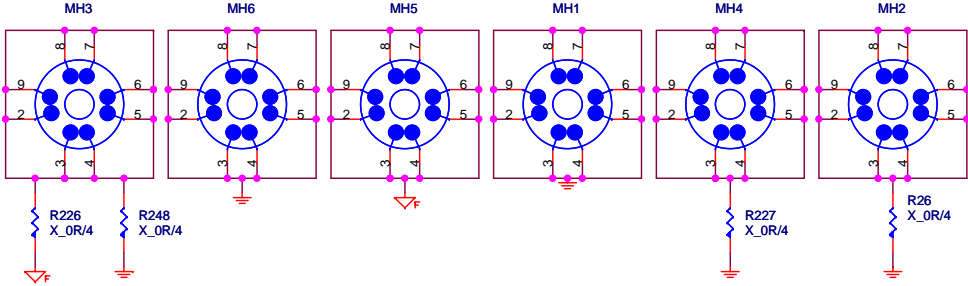
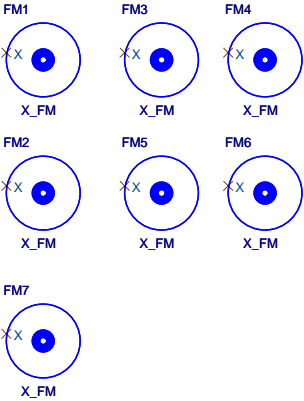


Title			
KB/MS,LPT,COM,Floppy CONN			
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Optics Orientation Holes

Mounting Holes

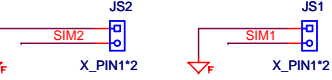


NB FAN/HEAT-SINK

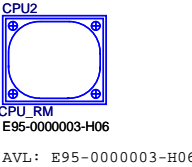
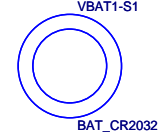
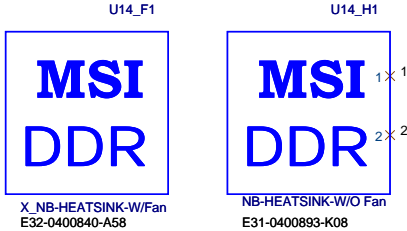
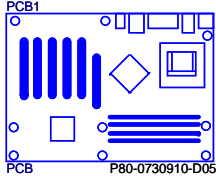
BATTERY

CPU RM

Simulation

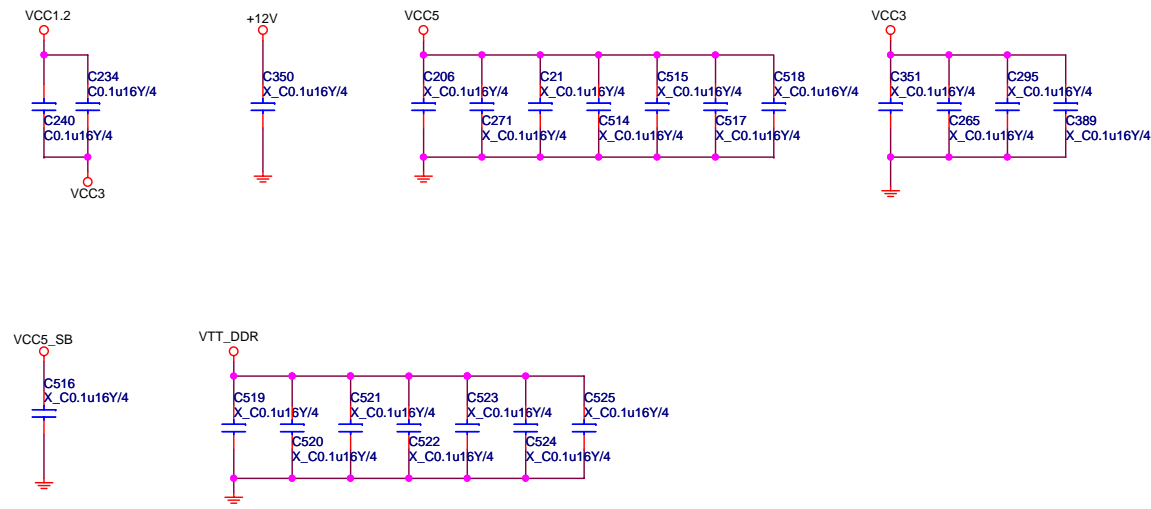


PCB



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For IDE BUS



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For EMI		
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2006/7/4

Split VCC1_2HT to VCC1_2HT & VCC1.2
Change USB_RBIAS_GND resister from 931ohm to 1.1K for DG(05) change
Change LPC_CLK termination resister from 22ohm to 33ohm for DG(04) change
don't stuff cap on LPC_CLK for DG(05) change
Change BUF_25MHZ to MII_PHY termination resister from 22ohm to 0ohm for DG(05) change
Change CLK200_TERM_GND resister from 562ohm to 2.37K for DG(05) change

2006/7/5

Change DAC_RSET resister from 124ohm to 105ohm for better signal

2006/7/6

Update l394 circuit for VIA FAE recommend

2006/7/7

Update Audio circuit for Vista

Title		
HISTORY		
Size	Document Number	Rev
	MS-7309	0A
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ATX P/S WITH 1A STBY CURRENT						CPU PW
VBAT	5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%	12V +/-5%

VRM SW
REGULATOR

CPU_VCORE (S0, S1)

VDD 1.5V
REGULATOR

VDD 1.2V
REGULATOR

AM2 ATHLON 64	
VCORE 0.8-1.55V 80A(90W)	VTT_DDR 1.75A
	VCC_DDR 3.6A
	VCC1_2HT 1.2V 0.5A

VTT_DDR(S0,S1,S3)	
VCC_DDR(S0,S1,S3)	
VCC1_2HT (S0, S1)	

VCC1_2HT(S0,S1)

MCP61	
VCC1_2HT 7.5A	
VCC3 0.615A	
3VDUAL 0.556A	
1.2VDUAL 0.225A	
VBAT 5mA(S0,S1)/ 100uA(S3,S5)/ 10uA(G3)	

0.9V VTT_DDR
REGULATOR

1.8V VCC_DDR
REGULATOR

VTT_DDR(S0,S1,S3)

VCC_DDR(S0,S1,S3)

DDR400 DIMMs	
VTT_DDR 0.3A/DIMM (0.6A)	
VCC_DDR 2.6A/DIMM (5.2A)	

3VDUAL (S0, S1, S3, S4, S5)

1.2VDUAL (S0, S1, S3, S4, S5)

VBAT(G3,S0,S1,S3,S4,S5)

+3.3VDUAL REGULATOR
ACPI CONTROLLER

3VDUAL (S0, S1, S3, S4, S5)

+5VSB REGULATOR
ACPI CONTROLLER

+5V_Dual (S0, S1, S3)

1.2V STB
REGULATOR

1.2VDUAL (S0, S1, S3, S4, S5)

VCC3 (S0, S1)

VBAT(G3,S0,S1,S3,S4,S5)

5VAA LDO
REGULATOR

+5VR (S0, S1)

VCC3 (S0, S1)

+5VR (S0, S1)

3VDUAL (S0, S1, S3, S4, S5)

3VDUAL (S0, S1, S3, S4, S5)

VCC3 (S0, S1)

VBAT

+5V_Dual (S0, S1, S3)

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X2

+3.3VDUAL (S0, S1, S3)

X1 PCIE		X16 PCIE	
3.3V	3.0A	3.3V	3.0A
12V	5.5A	12V	5.5A

1394 FR*1	1394 RL*1
12V 1.5A	12V 1.5A

USB FR*4
5VDual 2A

USB RL*4
5VDual 2A

PS/2
5VDual 1A